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1. **VON NEUMANN ARCHITECTURE**

Von-Neumann architecture has the following basic characteristics:

• Consists of three hardware systems: A central processing unit (CPU) (which consists of a control unit, an arithmetic logic unit (ALU), registers (small storage areas), and a program counter);

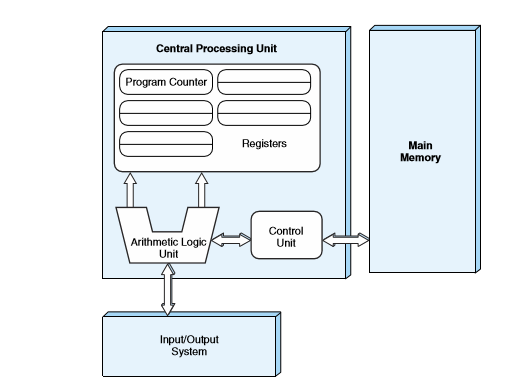
a main-memory system, which holds programs that control the computer’s operation; and

an I/O system.

• Capacity to carry out sequential instruction processing

• Contains a single path, either physically or logically, between the main memory system and the control unit of the CPU, forcing alternation of instruction and execution cycles. This single path is often referred to as the von Neumann bottleneck.

MODE OF OPERATION



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1. The control unit fetches the next program instruction from the memory, using the program counter to determine where the instruction is located.

2. The instruction is decoded into a language the ALU can understand.

3. Any data operands required to execute the instruction are fetched from memory and placed into registers within the CPU.

4. The ALU executes the instruction and places the results in registers or memory

1. AMD

Long ago, AMD was a second-source supplier for Intel, AMD first focused on producing logic chips. The company guaranteed quality control to United States Military Standard, an advantage in the early computer industry since unreliability in microchips was a distinct problem that customers – including computer manufacturers,

in 1974 it was actually a little bit of corporate subterfuge that led AMD to produce its first ever CPU the am98 which was essentially a clone of intel 8080 that AMD reversed engineering The two chip makers came into an agreement that had AMD manufacture intel designed CPU Symbiotic relationship began to share technology with each other as they compete in the market for each other

intel licensed the x86 architecture to AMD in 91976 which made AMD design compatible CPU to this. AMD cloned 386 intel processor, as the part of the agreement its then they realized they had to design own CPU in house their own k5 was made to that compete with Pentium with clock speed 136 mg in 1996

AMD launched a chip that made them become major as they designed k6 that compete with Pentium 2 and 3 that gave better performance in gaming and multimedia

**C) SPARC** stands for Scalable Processor Architecture

**SPARC** was designed as a target for optimizing compilers and easily pipelined hardware implementations. SPARC implementations provide exceptionally high execution rates (MIPS) and short time-to-market development schedules.

Provide the scalability of the cost/performance ratio of successive implementations with the current improvements in circuit technology.

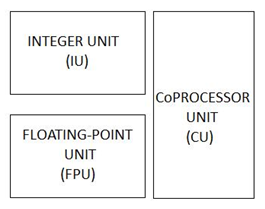
The "Scalable" in **SPARC** comes from the fact that the SPARC specification allows implementations to scale from processors required in embedded systems to processors used for servers.

It is a Load and store architecture. Operations are always done over registers.

Uses “register window” concept thus offering a large number of registers.

Uses delay slot to optimize branch instruction.

Passes arguments using registers and the stack.



**Integer Unit**

Contains the general-purpose registers and controls the overall operation of the processor.

It may contain from 64 to 528 general-purpose 64-bit r registers. They are partitioned into 8 global registers, 8 alternate global registers, plus a circular stack of from 3 to 32 sets of 16 registers each, known as register windows.

Executes the integer arithmetic instructions and computes memory addresses for loads and stores. -Maintains the program counters and controls instruction execution for the FPU.

**Floating Point Unit**

The FPU has 32-bit (single-precision) floating-point registers, 64-bit (double-precision) floating-point registers, and 128-bit (quad-precision) floating-point registers.

Double-precision values occupy an even-odd pair of single-precision registers.

Quad-precision values occupy an odd-even number pair of double precision registers.

Floating-point load/store instructions are used to move data between the FPU and memory.

The memory address is calculated by the IU.

Floating-Point operate instructions perform the floating-point arithmetic operations and comparisons.

**Coprocessor Unit**

The instruction set includes support for a single, implementation-dependent coprocessor. The coprocessor has its own set of registers.

Coprocessor load/store instructions are used to move data between the coprocessor registers and memory floating-point instructions mirrors coprocessor instructions.